111. (New) The method of Claim 110, wherein the optimizing step is performed through the dynamic programming technique.

112 ~~113.~~ (New) The method of Claim ~~112,~~ 111 wherein the detailed placement process further comprises the step of performing a greedy cleanup process.

113 ~~114.~~ (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a single row optimally according to a sum of squares objective in linear, quadratic, or polynomial run time.

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~~115.~~ (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a single row optimally for a given fixed cell ordering in linear, quadratic, or polynomial run time.

115

~~116.~~ (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

legalizing a single row optimally using a dynamic programming technique for the swapping of cells between the pairs of rows based on the cost function.

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116
~~117.~~ (New) A method for placing cells of a netlist, comprising the steps of:

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receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby

allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes two rows optimally according to a sum of squares objective in quadratic or polynomial run time.

117

~~118.~~ (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes two rows optimally for a given fixed cell ordering in quadratic or polynomial run time.

118

~~119.~~ (New) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

legalizing two row optimally using a dynamic programming technique for the swapping of cells between the pairs of rows based on the cost function.

119

~~120.~~ (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a pair of rows optimally according to y-displacement metric in quadratic or polynomial time.

120

~~121~~. (New) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby

allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes N rows optimally according to a y-displacement metric in quadratic or polynomial run time.